SDEC

DOT MATRIX
LIQUID CRYSTAL DISPLAY
MODULE

LMG-SSC14A32 Serial

USER‘ MANUAL

	LMG-SSC14A32DRG		**LMG-SSC14A32DRY**
	LMG-SSC14A32DLGY		**LMG-SSC14A32DLYY**
	LMG-SSC14A32DLGY-E		**LMG-SSC14A32DLYY-E**

PROPOSED BY		**APPROVED**
Design	Approved	

SDEC TECHNOLOGY CORP.

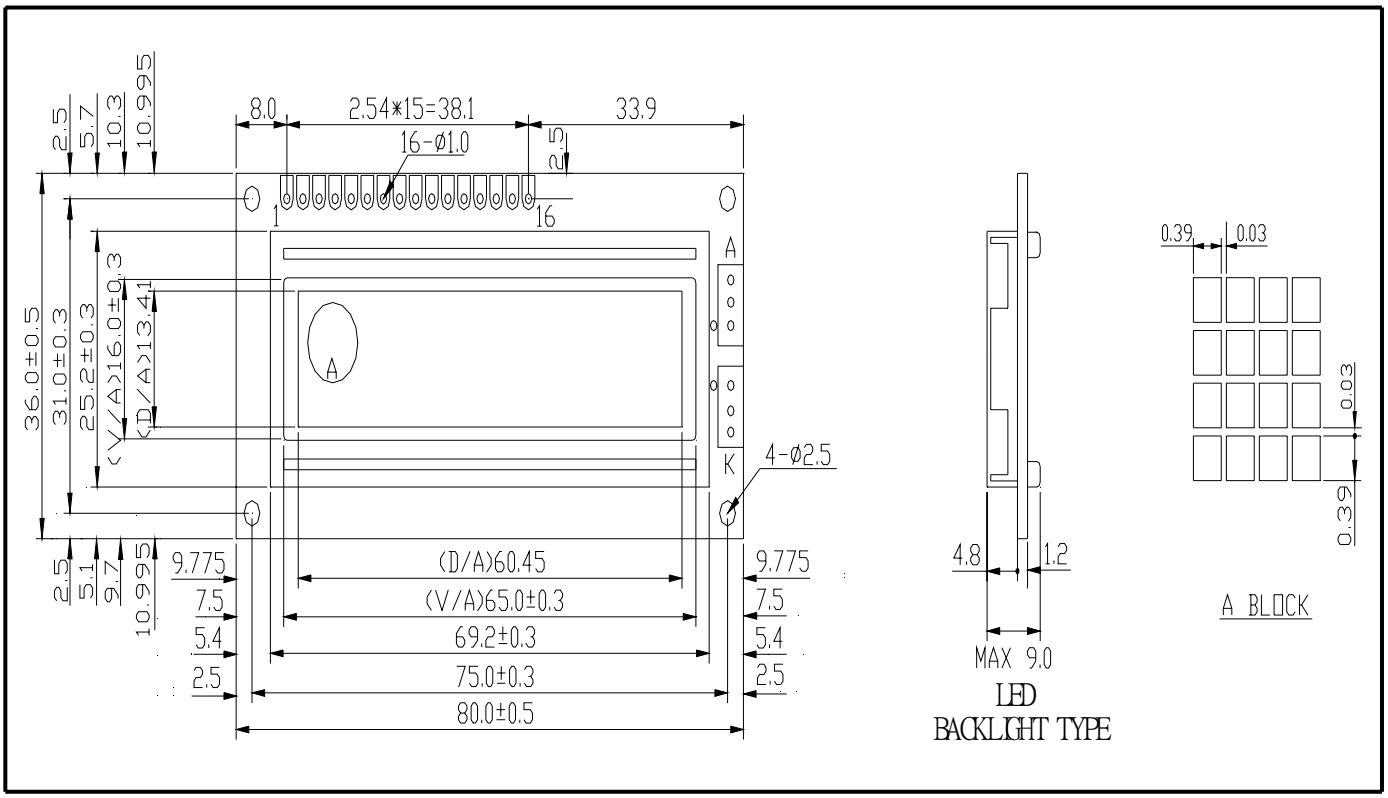
CONTENTS

		PAGE
1.	**Mechanical Specification**	**2**
2	**Mechanical Diagram**	**2**
3.	**Interface Pin Connections**	**2**
4.	**Absolute Maximum Rating**	**3**
5.	**Electrical Characteristics**	**3**
6.	**Optical Characteristics**	**3**
7.	**Optical Definitions**	**3**
8.	**Char Display Address**	**3**
9.	**Interface to MPU**	**4**
	9.1 Interface to Z-80 CPU	**4**
	9.2 Interface to MC6800 CPU	**4**
	9.3 Interface to 4-bit CPU (HMCS43C)	**4**
	9.4 Interface to HD6805 MP	**4**
10.	**Timing Control**	**4**
	10.1 Write and Read Operation	**4**
	10.2 Busy flag check timing	**4**
11.	**Initialization of LCM**	**5**
12.	**Instruction Set**	**6**
13.	**User Font Patterns**	**7**
14.	**Icon RAM Data**	**7**
15.	**Graph Display RAM Address**	**8**
16.	**Software Example**	**8**
	16.1 8-bit operation (8 bits 2 lines)	**8**
	16.2 4-bit operation (4 bits 2 lines)	**8**
17.	**Reliability Condition**	**9**
18.	**Function Test & Inspection Criteria**	**9**
19	**Character Generator ROM Map**	**10**

1. Mechanical Specification

ITEM	STANDARD VALUE			UNIT
NUMBER OF CHARACTERS	9 CHARACTERS X 2 LINES (16*16 中文字)			--
CHARACTER FORMAT	16 X 16 DOTS			--
MODULE DIMENSION	80.0 (W) X 36.0 (H) X 9.0 (T)	80.0 (W) X 36.0 (H) X 13.2 (T)		mm
VIEWING DISPLAY AREA	65.0 (W) X 16.0 (H)			mm
ACTIVE DISPLAY AREA	60.45 (W) X 13.41 (H)			mm
DOT SIZE	0.39 (W) X 0.39 (H)			mm
DOT PITCH	0.42 (W) X 0.42 (H)			mm
LMG-SSC14A32DRG	STN , Gray , 1/32 Duty , 6 O'clock			
LMG-SSC14A32DRY	STN , Yellow Green , 1/32 Duty , 6 O'clock			
LMG-SSC14A32DLGY	STN , Gray , 1/32 Duty , 6 O'clock , LED Backlight			
LMG-SSC14A32DLYY	STN , Yellow Green , 1/32 Duty , 6 O'clock , LED Backlight			
LMG-SSC14A32DLGY-E	STN , Gray , 1/32 Duty , 6 O'clock , E Mode LED Backlight			
LMG-SSC14A32DLYY-E	STN , Yellow Green , 1/32 Duty , 6 O'clock , E Mode LED Backlight			
LED Backlight Color	Yellow Green			
LED Backlight Input	DC +5V	V	100	mA
Backlight Half-Lift Time	50,000			HR.
E Mode LED Backlight Color	Yellow Green			
E Mode LED Backlight Input	DC +5V	V	40	mA
E mode Backlight Half-Lift Time	30,000			HR.

2. Mechanical Diagram



3. Interface Pin Connections

NO	SYMBOL	LEVEL	FUNCTION	NO	SYMBOL	LEVEL	FUNCTION
1	VSS	--	GND (0V)	9	DB2	H/L	Data Bit 2
2	VDD	H/L	DC +5V	10	DB3	H/L	Data Bit 3
3	N.C	--	N.C	11	DB4	H/L	Data Bit 4
4	RS	H/L	Register select	12	DB5	H/L	Data Bit 5
5	R/W	H/L	Read/Write	13	DB6	H/L	Data Bit 6
6	E	H,H→L	Enable signal	14	DB7	H/L	Data Bit 7
7	DB0	H/L	Data Bit 0	15	A(+)	DC +5V	LED Backlight +
8	DB1	H/L	Data Bit 1	16	K(-)	0V	LED Backlight -

4. Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYPE	MAX.	UNIT
OPERATING TEMPERATURE	TOP	0	--	+50	℃
STORAGE TEMPERATURE	TST	-10	--	+60	℃
INPUT VOLAGE	VI	VSS	--	VDD	V
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	--	5.0	6.5	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	--	--	6.5	V
STATIC ELECTRICITY	Be sure that you are grounded when handing LCM.				

5. Electrical Characteristics

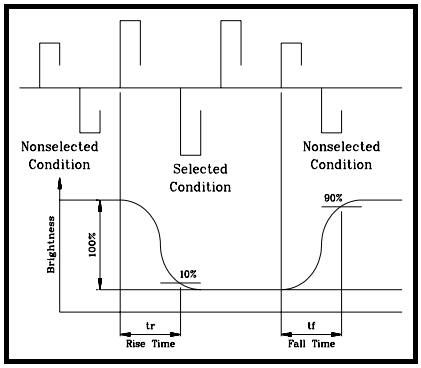
ITEM	SYN	CONDITION	MIN.	TYPE	MAX.	UNIT
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	--	4.5	5.0	5.5	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	Ta= 0 ℃	--	6.1	--	V
		Ta= +25 ℃	--	5.8	--	V
		Ta= +50 ℃	--	5.5	--	V
INPUT HIGH VOLTAGE	VIH	--	2.2	--	VDD	V
INPUT LOW VOLTAGE	VIL	--	0	--	0.6	V
OUTPUT HIGH VOLTAGE	VOH	--	2.4	--	--	V
OUTPUT LOW VOLTAGE	VOL	--	--	--	0.4	V
SUPPLY CURRENT	IDD	VDD=+5V	--	3.0	4.5	mA

6. Optical Characteristics

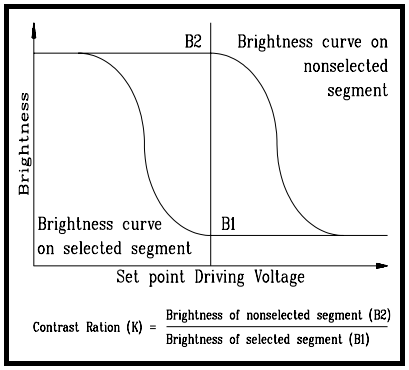
ITEM	SYM	CONDITION	MIN.	TYPE	MAX.	UNIT
VIEW ANGLE (V)	θ	CR≧2	-10	--	40	deg.
VIEW ANGLE (H)	φ	CR≧2	-30	--	30	deg.
CONTRAST RATIO	CR	--	--	5	--	--
RESPONSE TIME	TON	--	--	180	230	mS
RESPONSE TIME	TOFF	--	--	100	150	mS

7. Optical Definitions

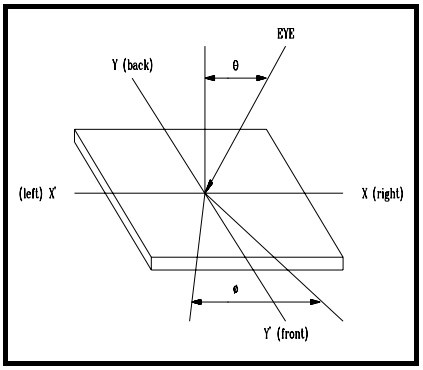
Response Time



Contrast Ration


B2
Brightness curve on nonselected segment
Brightness
Brightness curve on selected segment
B1
Set point Driving Voltage
Contrast Ration (K) = Brightness of nonselected segment (B2) / Brightness of selected segment (B1)

View Angle



8. Char Display Address

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80H		81H		82H		83H		84H		85H		86H		87H	
Line 2	90H		91H		92H		93H		94H		95H		96H		97H	
Line 3																
Line 4																

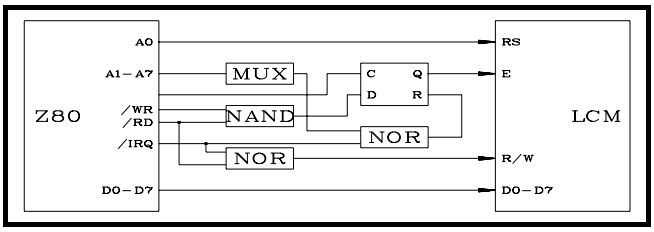
	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Line 1	88H															
Line 2	98H															
Line 3																
Line 4																

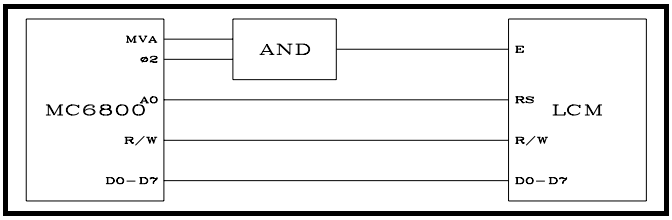
*A Ram Bank is 16 bits (2 bytes)

9. Interface to MPU

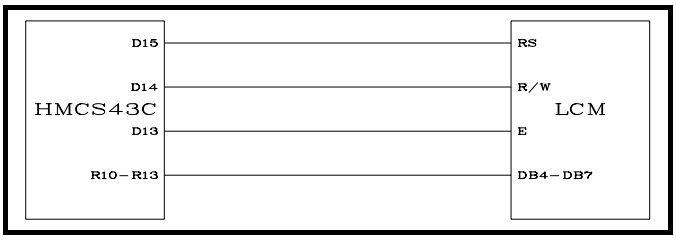
9.1 Interface to Z-80 CPU

9.2 Interface to MC6800 CPU

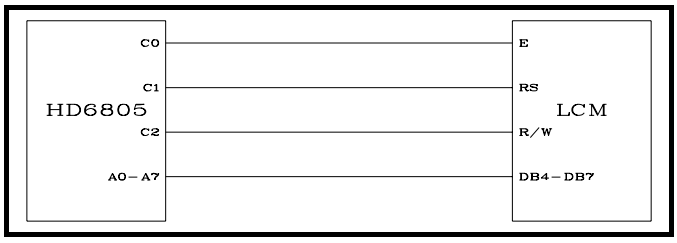




9.3 Interface to 4-bit CPU (HMCS43C)



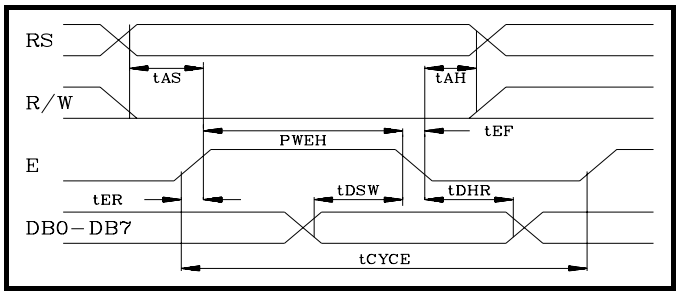
9.4 Interface to HD6805 MP



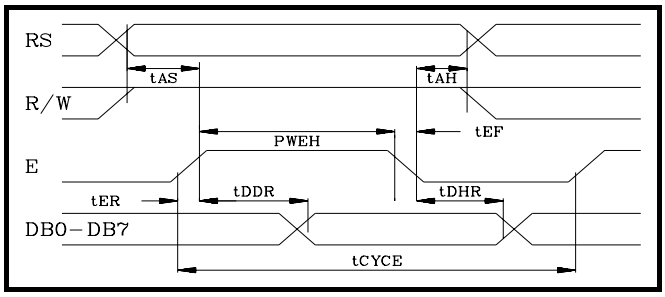
10. Timing Control

10.1 Write and Read Operation

Write Operation

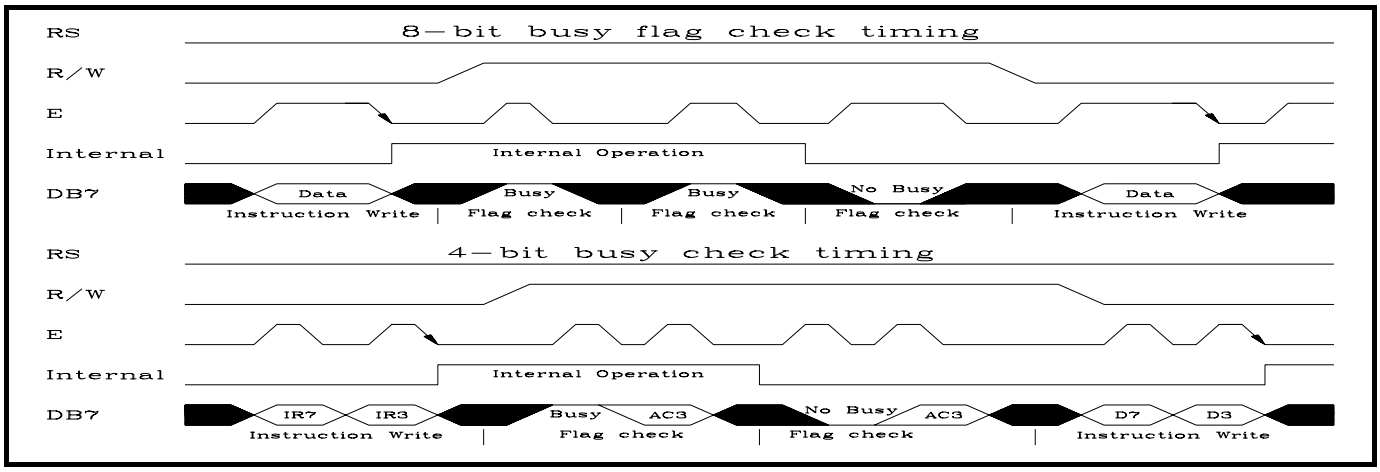


Read Operation



Item	Symbol	Limit (Min.)	Limit (Max.)	Unit
Enable Cycle Time	tCYCE	1200	--	ns
Enable Pules Width (High level)	PWEH	140	--	ns
Enable Rise/Fall Time	tER,tEF	--	25	ns
Address Set-Up Time (RS,R/W,E)	tAS	10	--	ns
Address Hole Time	tAH	20	--	ns
Data Set-Up Time	tDSW	40	--	ns
Data Delay Time	tDDR	--	100	ns
Data Hold Time	tDHR	20	--	ns

10.2 Busy flag check timing



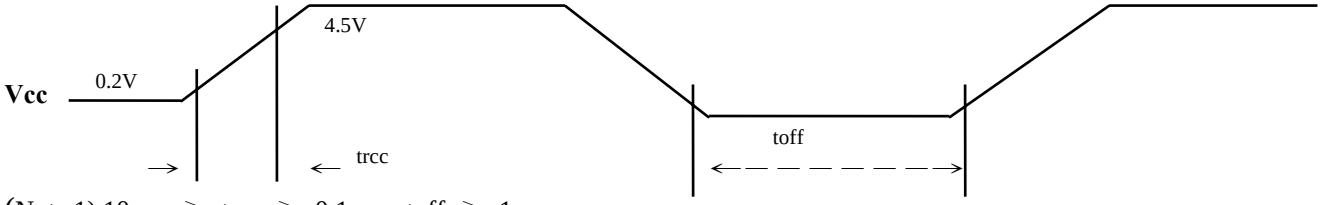
Note : IR7, IR3 : Instruction 7th bit , 3rd bit ; AC3 : Address Counter 3rd bit.

11. Initialization of LCM

The LCM automatically initializes (reset) when power is turned on using the internal reset circuit. If the power supply

conditions for correctly operating of the internal reset circuit are not met, initialization by instruction is required. Use the procedure is next page for initialization.

Internal Power Supply reset



(Note 1) 10 ms ≧ trcc ≧ 0.1 ms , toff ≧ 1 ms.
(Note 2) toff stipulates the time of power OFF for momentary power supply dip or when power supply cycles ON and OFF.

Item	Symbol	Test condition	Limit (Min.)	Limit (Max.)	Unit
Power supply rise time	trcc	--	0.1	10	ms
Power supply off time	toff	--	1	--	ms

8 bit Interface

Power On

Wait time > 40 ms

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	0	X	X

Wait time > 100 μs

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	0	X	X

Wait time > 37 μs

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Wait time > 100 μs

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Wait time > 10ms

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Initialization End

4 bit Interface

Power On

Wait time > 40 ms

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	X	X	X	X

Wait time > 100 μs

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	X	X	X	X
0	0	X	0	X	X	X	X	X	X

Wait time > 100 μs

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	1	D	C	B	X	X	X	X

Wait time > 100 μs

Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	0	0	1	X	X	X	X

Wait time > 10ms

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	X	X	X	X
0	0	0	1	I/D	S	X	X	X	X

Initialization End

12. Instruction Set

Instruction Table: (RE=0: Enable basic instruction.)

Instruction	Instruction Code										Description	Ex. Time 540KHz
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear entire display and return the cursor to home position (address 0).	4.6ms
Return Home	0	0	0	0	0	0	0	0	1	X	Return cursor to the home position. Also returns the display being shifted to the original position. DDRAM contents remain unchanged.	4.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operation are performed during data rite/read. For normal operation. I/D=1 : increment ; 0 :decrement ; S=1 : accompanies display shift when data is written, for normal operation, set to zero.	72 μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	D=1: ON display ; 0:OFF display. C=1: ON cursor ; 0: OFF cursor. B=1: ON blink cursor ; 0: OFF blink cursor.	72 μs
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	X	X	S/C=1: Display shift; 0:Cursor move. R/L=1: shift to right; 0: shift to left.	72 μs
Function Set (Modify)	0	0	0	0	1	DL	X	0 RE	X	X	DL=1: Interface is 8 bits. 0: Interface is 4 bits. RE=0: Normal instruction .1: Extended instruction.	72 μs
Set CGRAM address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	72 μs
Set DDRAM address	0	0	1	0	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	72 μs
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM. (DDRAM/CGRAM/IRAM/GRAM)	72 μs
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM. (DDRAM/CGRAM/IRAM/GRAM)	72 μs

Instruction Table (RE=1: Enable extension instruction.)

Instruction	Instruction Code										Description	Ex. Time 540KHz
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Standby Mode	0	0	0	0	0	0	0	0	0	1	Enter standby mode, only Icon areas display Standby mode can be released by any other instructions.	72 μs
Start Row Enable	0	0	0	0	0	0	0	0	1	SR	SR=1: Allow change start display Row. SR=0: Disable start display Row change.	72 μs
Reverse Line select	0	0	0	0	0	0	0	1	R1	R0	Choice one of 4 line which data is reverse display.	72 μs
Sleep mode and set GRAM page	0	0	0	0	0	0	1	SL	X	X	SL=0:Enter sleep mode. 1:Wake-up from sleep mode	72 μs
Function Set (Modify)	0	0	0	0	1	DL	X	1 RE	G	0	DL=1: Interface is 8 bits. 0: Interface is 4 bits. RE=1: Extended instruction.0: Normal instruction. G=1: Graphic display ON. 0: Graphic display OFF	72 μs
Set Iram/Start Row address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	SR=1: AC5 – AC0 is start Row. SR=0: AC3 – AC0 is ICON RAM address.	72 μs
Set Graphic RAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set GDRAM address in address counter. Execute once set the address of display row (AC6-AC0). Execute again set the address of display column (AC3-AC0).	72 μs
				0	0	0	AC3	AC2	AC1	AC0		

13. User Font Patterns (CG RAM Character)

Character Code (DDRAM data)	CGRAM Address	CGRAM data (High byte)	CGRAM data (Low byte)

B15 – B4	B3	B2	B1	B0	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	X	00		X	00		0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0
							0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0
							0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
							0	0	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	0
							0	1	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0
							0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0
							0	1	1	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1	0
							0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0
							1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0
							1	0	0	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	0
							1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0
							1	0	1	1	0	1	0	0	1	0	0	1	0	0	0	0	1	0	0	0
							1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
							1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
							1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	X	01		X	01		0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0
							0	0	0	1	0	0	1	0	0	0	0	1	0	1	0	1	0	1	0	0
							0	0	1	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	0	0
							0	0	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0
							0	1	0	0	1	0	1	0	1	0	0	0	1	1	1	1	1	0	0	0
							0	1	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
							0	1	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0
							0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0
							1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0
							1	0	0	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0
							1	0	1	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0
							1	0	1	1	1	0	1	0	1	0	0	0	1	1	1	1	1	0	0	0
							1	1	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0
							1	1	0	1	0	0	1	1	1	0	0	0	0	0	1	0	0	0	0	0
							1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
							1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14. Icon RAM Data

Icon RAM Address				Icon RAM Data															
				High Byte								Low Byte							
AC3	AC2	AC1	AC0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Seg0	Seg1	Seg2	Seg3	Seg4	Seg5	Seg6	Seg7	Seg8	Seg9	Seg10	Seg11	Seg12	Seg13	Seg14	Seg15
0	0	0	1	Seg16	Seg17	Seg18	Seg19	Seg20	Seg21	Seg22	Seg23	Seg24	Seg25	Seg26	Seg27	Seg28	Seg29	Seg30	Seg31
0	0	1	0	Seg32	Seg33	Seg34	Seg35	Seg36	Seg37	Seg38	Seg39	Seg40	Seg41	Seg42	Seg43	Seg44	Seg45	Seg46	Seg47
0	0	1	1	Seg48	Seg49	Seg50	Seg51	Seg52	Seg53	Seg54	Seg55	Seg56	Seg57	Seg58	Seg59	Seg60	Seg61	Seg62	Seg63
0	1	0	0	Seg64	Seg65	Seg66	Seg67	Seg68	Seg69	Seg70	Seg71	Seg72	Seg73	Seg74	Seg75	Seg76	Seg77	Seg78	Seg79
0	1	0	1	Seg80	Seg81	Seg82	Seg83	Seg84	Seg85	Seg86	Seg87	Seg88	Seg89	Seg90	Seg91	Seg92	Seg93	Seg94	Seg95
0	1	1	0	Seg96	Seg97	Seg98	Seg99	Seg100	Seg101	Seg102	Seg103	Seg104	Seg105	Seg106	Seg107	Seg108	Seg109	Seg110	Seg111
0	1	1	1	Seg112	Seg113	Seg114	Seg115	Seg116	Seg117	Seg118	Seg119	Seg120	Seg121	Seg122	Seg123	Seg124	Seg125	Seg126	Seg127
1	0	0	0	Seg128	Seg129	Seg130	Seg131	Seg132	Seg133	Seg134	Seg135	Seg136	Seg137	Seg138	Seg139	Seg140	Seg141	Seg142	Seg143
1	0	0	1	Seg144	Seg145	Seg146	Seg147	Seg148	Seg149	Seg150	Seg151	Seg152	Seg153	Seg154	Seg155	Seg156	Seg157	Seg158	Seg159
1	0	1	0	Seg160	Seg161	Seg162	Seg163	Seg164	Seg165	Seg166	Seg167	Seg168	Seg169	Seg170	Seg171	Seg172	Seg173	Seg174	Seg175
1	0	1	1	Seg176	Seg177	Seg178	Seg179	Seg180	Seg181	Seg182	Seg183	Seg184	Seg185	Seg186	Seg187	Seg188	Seg189	Seg190	Seg191
1	1	0	0	Seg192	Seg193	Seg194	Seg195	Seg196	Seg197	Seg198	Seg199	Seg200	Seg201	Seg202	Seg203	Seg204	Seg205	Seg206	Seg207
1	1	0	1	Seg208	Seg209	Seg210	Seg211	Seg212	Seg213	Seg214	Seg215	Seg216	Seg217	Seg218	Seg219	Seg220	Seg221	Seg222	Seg223
1	1	1	0	Seg224	Seg225	Seg226	Seg227	Seg228	Seg229	Seg230	Seg231	Seg232	Seg233	Seg234	Seg235	Seg236	Seg237	Seg238	Seg239
1	1	1	1	Seg240	Seg241	Seg242	Seg243	Seg244	Seg245	Seg246	Seg247	Seg248	Seg249	Seg250	Seg251	Seg252	Seg253	Seg254	Seg255

15. Graph Display RAM Address

GDRAM Column Address	GDRAM Row Address			
	0	1	-----	15
0	D15 → D0	D15 → D0	D15 → D0	D15 → D0
1	D15 → D0	D15 → D0	D15 → D0	D15 → D0
2	D15 → D0	D15 → D0	D15 → D0	D15 → D0
:	:	:	:	:
61	D15 → D0	D15 → D0	D15 → D0	D15 → D0
62	D15 → D0	D15 → D0	D15 → D0	D15 → D0
63	D15 → D0	D15 → D0	D15 → D0	D15 → D0

16. Software Example

16.1 8-bit operation (8 bits 2 lines)

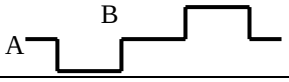
Function	RS	RW	D7	D6	D5	D4	D3	D2	D1	D0	Display	Description
Power on delay												Initialization. No display appears.
Function set	0	0	0	0	1	1	0	0	0	0		Sets to 8-bit operation and selects 2-line display character font. (Note: number of display lines and character fonts cannot be change after this.)
Display OFF	0	0	0	0	0	0	1	0	0	0		Turn off display.
Display ON	0	0	0	0	0	0	1	1	1	0	_	Turn on display and cursor
Entry Mode Set	0	0	0	0	0	0	0	1	1	0	_	Set mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM Display is not shifted.
Write data to CG/DD RAM	1 1	0 0	1 1	0 0	1 1	1 0	0 1	1 1	1 1	0 1	雄_	Write “雄”. Cursor incremented by one and shift to right.
Write data to CG/DD RAM	1 1	0 0	1 0	1 1	0 0	0 0	0 1	1 1	0 0	1 1	雄鐸_	Write “鐸” .
Set DD RAM	0	0	1	0	0	1	0	0	0	0	雄鐸 _	Set RAM address so that the cursor is propositioned at the head of the second line.
Write data to CG/DD RAM	*	*									雄鐸 CR_	Write “C” , and “R”.
Cursor or display shift	0	0	0	0	0	1	0	0	x	x	雄鐸 CR_	Shift only the cursor position to the left.
Write data to CG/DD RAM	*	*									雄鐸 CO., LTD._	Write “O., LTD.” .
Entry Mode Set	0	0	0	0	0	0	0	1	1	1	雄鐸 CO., LTD._	Set display mode shift at the time during writing operation.
Write data to CG/DD RAM	1	0	0	1	1	1	1	0	0	0	鐸 ., LTD. x_	Write “ x”. Cursor incremented by one and shift to right. (The display move to left.)
Write data to CG/DD RAM	*	*										Write other characters.
Return Home	0	0	0	0	0	0	0	0	1	0	雄鐸 CO., LTD.	Return both display and cursor to the original position (Set address to zero).

16.2 4-bit operation (4-bit, 1 line)

Function	RS	R/W	D7	D6	D5	D4	Display	Description
power on delay								initialization. No display appears.
Function set	0	0	0	0	1	0		Sets to 4-bit operation. In this case, operation is handled as 8-bits by initialization, and only this instruction completes with one write.
Function set	0 0	0 0	0 0	0 0	1 0	0 0		Sets 4-bit operation and selects 1-line display character font on and resetting is needed. (number of display lines and character fonts cannot be changed hence after).
Display ON/OFF Control	0 0	0 0	0 1	0 1	0 1	0 0	_	Turn on display and cursor.
Entry Mode Set	0 0	0 0	0 0	0 1	0 1	0 0	_	Set mode to incremented the address by one and to shift the cursor to the right, at the time of write. to the DD/CG RAM display is not shifted.
Write data to CG/DD RAM	1 1 1 1	0 0 0 0	1 0 1 1	0 1 0 1	1 1 1 1	1 0 0 1	雄_	Write “雄”. Cursor incremented by one and shift to right.
same as 8-bit operation								

17. Reliability Condition

TN Type	STN Type

			Normal Temp.	Wide Temp.	Normal Temp.	Wide Temp.
Viewing Angle	Horizontal Φ		±30°	±30°	±30°	±30°
	Vertical Θ(㎜)		10° to 30°	10° to 30°	-10° to 40°	-10° to 40°
Operating Temperature			-10 to 70℃	-25 to 80℃	0 to 50℃	*-20 to 70℃
Storage Temperature			-20 to 80℃	-35 to 90℃	-20 to 70℃	*-30 to 80℃
High Temperature (Power Off)			240 Hours @70℃	240 Hours @90℃	240 Hours @65℃	240 Hours @75℃
Low Temperature (Power Off)			240 Hours @-20℃	240 Hours @-35℃	240 Hours @-15℃	240 Hours @-25℃
High Temperature (Power On)			240 Hours @70℃	240 Hours @80℃	240 Hours @60℃	240 Hours @70℃
Low Temperature (Power On)			240 Hours @-10℃	240 Hours @-25℃	240 Hours @-10℃	240 Hours @-20℃
High Temperature & High Humidity			55℃/90%RH 240 Hours	75℃/90%RH 240 Hours	45℃/90%RH 240 Hours	65℃/90%RH 240 Hours
Thermal Shock 5 Cycle 		A	60min@-20℃	60min@-35℃	60min@-20℃	60min@-30℃
		B	5min@25℃	5min@25℃	5min@25℃	5min@25℃
		C	60min@70℃	60min@90℃	60min@70℃	60min@80℃
Expected Lift			50,000 Hours	50,000 Hours	50,000 Hours	50,000 Hours

*Wide temp. version may not available for some products, Please consult our sales engineer or respresentative.

18. Functional Test & Inspection Criteria

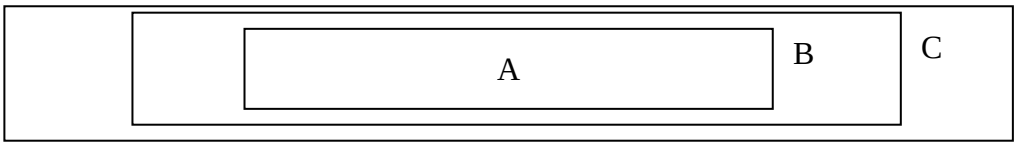
18.1 Sample plan

Sample plan according to MIL-STD-105D level 2, and acceptance/rejection criteria is.
Base on : Major defect : AQL 0.65 Minor defect : AQL 2.5

18.2 Inspection condition

Viewing distance for cosmetic inspection is 30cm with bare eyes, and under an environment of 800 lus (20W) light intensity. All direction for inspecting the sample should be within 45° against perpendicular line.

18.3 Definition of Inspection Zone in LCD



Zone A : Character / Digit area
Zone B : Viewing area except Zone A (Zone A + Zone B = minimum Viewing area)
Zone C : Outside viewing area (invisible area after assembly in customer's product)
Note : As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.

18.4 Major Defect

All functional defects such as open (or missing segment), short, contrast differential, excess power consumption, smearing, leakage, etc. and overall outline dimension beyond the drawing. Are classified as major defects.

18.5Minor Defect

Except the Major defects above, all cosmetic defects are classified as minor defects.

<table>
<tr><th>Item No.</th><th>Item to be Inspected</th><th colspan="5">Inspection Standard</th><th>Classification of defects</th></tr>
<tr><td rowspan="6">1.</td><td rowspan="6">Spot defect
(Defects in spot from)</td><td rowspan="2">Zone size (mm)</td><td colspan="3">Acceptable Qty</td><td rowspan="6">Minor</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ ≦0.15</td><td colspan="2">Acceptable (clutering of spot not allowed)</td><td>Accepta-ble</td></tr>
<tr><td>0.15≦ Φ ≦0.20</td><td>1</td><td>2</td><td rowspan="3"></td></tr>
<tr><td>0.20≦ Φ ≦0.25</td><td>0</td><td>1</td></tr>
<tr><td>Φ>0.25</td><td>0</td><td>0</td></tr>
<tr><td colspan="5">Remarks : for dark/white spot, size Φ is defined as Φ=1/2(X+Y)</td></tr>
<tr><td rowspan="8">2.</td><td rowspan="8">Line defect (Defects in line form)</td><td colspan="2">Size (mm)</td><td colspan="3">Acceptable Qty</td><td rowspan="8">Minor</td></tr>
<tr><td rowspan="2">L
Length</td><td rowspan="2">W
Width</td><td colspan="3">Zone</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Accep-table</td><td>W≦0.02</td><td colspan="2">Accep-table</td><td>Accep-table</td></tr>
<tr><td>L≦3.0</td><td>W≦0.03</td><td colspan="2">2</td><td rowspan="4"></td></tr>
<tr><td>L>2.5</td><td>W≦0.03</td><td colspan="2">0</td></tr>
<tr><td>L≦3.0</td><td>0.03<W≦0.05</td><td colspan="2">2</td></tr>
<tr><td>L>2.5</td><td>0.03<W≦0.05</td><td colspan="2">0</td></tr>
<tr><td></td><td>W>0.05</td><td colspan="3">Counted as spot defect (Follows item 18.5.1)</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed four.</td></tr>
<tr><td>3.</td><td>Orientation defect (such as misalignment of L/C)</td><td colspan="5">Not allowed inside viewing area (Zone A or Zone B)</td><td>Minor</td></tr>
<tr><td rowspan="6">4.</td><td rowspan="6">Polarizing</td><td colspan="5">18.5.4.1 Polarizer Position
1. Shifting in Position Should not exceed the glass outline dimension.
2. Incomplete covering of the viewing area due to Shifting is not allowed.</td><td rowspan="6">Minor</td></tr>
<tr><td colspan="5">18.5.4.2 Seratches, bubble or dent on Glass/ Polarizer/Reflector, Bubble between Polarizer & Reflector/Glass:</td></tr>
<tr><td rowspan="2">Size (mm)</td><td colspan="3">Acceptable Qty</td><td rowspan="5">Accep-table</td></tr>
<tr><td colspan="3">Zone
A B C</td></tr>
<tr><td>Φ ≦0.20</td><td colspan="2">Acceptable</td></tr>
<tr><td>0.20<Φ ≦0.50</td><td colspan="2">3</td></tr>
<tr><td>0.50<Φ ≦1.00</td><td colspan="2">2</td></tr>
<tr><td>Φ>1.00</td><td colspan="2">0</td></tr>
</table>

19. Character Generator ROM Map

	Low 4-bit															
High 4-bit	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0			☻	♥	♦	♣	♠	•	◘	○	◙	♂	♀	♪	♫	☼
1	►	◄	↕	‼	¶	§	▬	↨	↑	↓	→	←	∟	↔	▲	▼
2		!	"	#	$	%	&	'	(	)	*	+	,	−	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	△

字型碼，前 127 碼為標準 ASCII 碼，在中文為半形，中文碼由 A140 開始，共 8192 字，編碼方式為 BIG-5 碼.

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